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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER
KIM, HONG CHONG

ART UNIT	PAPER NUMBER
2187	

DATE MAILED: 05/23/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/672,345	POISNER, DAVID I.
	Examiner	Art Unit
	Hong C Kim	2187

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 September 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 September 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

Detailed Action

1. Claims 1-30 are presented for examination. This office action is in response to the application filed on 9/28/00.

2. Applicants are reminded of the duty to disclose information under 37 CFR 1.56.

Specification

3. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed. The title should be more specific to differentiate the invention from similar inventions in the patent literature. It appears that embedded, integrated, or single chip aspects of the invention should be mentioned in the title so that the title is more descriptive.

Drawings

4. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, a flow diagram illustrating the logic implementation of accessing status and main memories must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held

in abeyance. No new matter should be entered.

Claim Objections

5. Claims 10-26 objected to because of the following informalities:

As to claims 10, 14, 19, and 23, it is unclear what is the difference between memory in line 2, memory in line 5 and memory in line 6 and memory in line 8.

As to claim 12, 17, 21, and 25, it is unclear what is the difference between memory in line 2 and memories in claim 10, 14, 19, and 23.

Appropriate correction is required.

Double Patenting

6. A rejection based on double patenting of the "same invention" type finds its support in the language of 35 U.S.C. 101 which states that "whoever invents or discovers any new and useful process ... may obtain a patent therefor ..." (Emphasis added). Thus, the term "same invention," in this context, means an invention drawn to identical subject matter. See *Miller v. Eagle Mfg. Co.*, 151 U.S. 186 (1894); *In re Ockert*, 245 F.2d 467, 114 USPQ 330 (CCPA 1957); and *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970).

A statutory type (35 U.S.C. 101) double patenting rejection can be overcome by canceling or amending the conflicting claims so they are no longer coextensive in scope. The filing of a

terminal disclaimer cannot overcome a double patenting rejection based upon 35 U.S.C. 101.

7. Claims 1-30 are provisionally rejected under 35 U.S.C. 101 as claiming the same invention as that of claims 1-30 of copending Application No. 09/572,047. This is a provisional double patenting rejection since the conflicting claims have not in fact been patented.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

9. Claims 1-6, 9, and 27-29 are rejected under 35 U.S.C. 102(e) as being anticipated by Camacho et al. (Camacho) US Patent 6,167,487.

As to claim 1, Camacho discloses the invention as claimed. Camacho discloses a computer system, comprising: a noncached multi-ported memory (Fig. 1 Ref. 12); a CPU

coupled to the multi-ported memory (col. 1 line 12); a peripheral device coupled to the multi-ported memory (col. 1 line 49); the CPU and the peripheral device being configured to access the multi-ported memory independently (col. 1 line 67).

As to claim 27, Camacho discloses the invention as claimed above. Camacho discloses integrated circuit comprising a memory controller including at least two electrical ports for coupling to communication channel (Fig. 1).

As to claim 2, Camacho discloses the invention as claimed above. Camacho further discloses an OS is configured such that accesses to the multiported are not cached (Fig. 1 Ref, 12).

As to claims 3 and 28, Camacho discloses the invention as claimed. Camacho further discloses the multi-ported memory is dual ported (Fig. 1).

As to claim 4, Camacho discloses the invention as claimed above. Camacho further discloses the multiported memory is embedded within a memory controller (Fig. 1 and col. 2 line 12).

As to claim 5, Camacho discloses the invention as claimed above. Camacho further discloses the multiported memory and memory controller are integrated into a single chip (Fig. 1

and col. 2 line 12).

As to claims 6 and 29 , Camacho discloses the invention as claimed above. Camacho further discloses DRAM (Fig. 1).

As to claim 9, Camacho discloses the invention as claimed above. Camacho further discloses I/O bus (Fig. 1).

Claim Rejections - 35 USC § 102

10. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

11. Claims 1-6, 9 and, 27-29 are rejected under 35 U.S.C. 102(b) as being anticipated by Csoppenszky et al. (Csoppenszky) US Patent 5,852,608.

As to claim 1, Csoppenszky discloses the invention as claimed. Csoppenszky discloses a computer system, comprising: a noncached multi-ported memory (Fig. 2 Ref. 201); a CPU coupled to the multi-ported memory (Fig. 2 Ref. 1 and col. 2 line 39); a peripheral device coupled to the multi-ported memory (Fig. 2 Ref. 2 and col. 2 line 43); the CPU and the peripheral

device being configured to access the multi-ported memory independently (col. 2 lines 37-45).

As to claim 27, Csoppenszky discloses the invention as claimed above. Csoppenszky integrated circuit comprising a memory controller including at least two electrical ports for coupling to communication channel (Fig. 2)

As to claim 2, Csoppenszky discloses the invention as claimed above. Csoppenszky further discloses an OS is configured such that accesses to the multiported are not cached (Fig. 2 Ref, 201).

As to claims 3 and 28, Csoppenszky discloses the invention as claimed. Csoppenszky further discloses the multi-ported memory is dual ported (Fig. 2 Ref. 201).

As to claim 4, Csoppenszky discloses the invention as claimed above. Csoppenszky further discloses the multiported memory is embedded within a memory controller (col. 2 lines 37-45).

As to claim 5, Csoppenszky discloses the invention as claimed above. Csoppenszky further discloses the multiported memory and memory controller are integrated into a single chip (col. 2 lines 37-45).

As to claims 6 and 29 , Csoppenszky discloses the invention as claimed above. Csoppenszky further discloses DRAM (col. 3 line 47-50).

As to claim 9, Csoppenszky discloses the invention as claimed above. Csoppenszky further discloses I/O bus (Fig. 2).

12. Claims 1-6, 9 and 27-29 are rejected under 35 U.S.C. 102(b) as being anticipated by Dinwiddie, Jr. et al. (Dinwiddie) US Patent 5,852,608.

As to claim 1, Dinwiddie discloses the invention as claimed. Dinwiddie discloses a computer system, comprising: a noncached multi-ported memory (Fig. 1 Ref. 22); a CPU coupled to the multi-ported memory (Fig. 1 Ref. 1); a peripheral device coupled to the multi-ported memory (Fig. 1 Ref. 3; the CPU and the peripheral device being configured to access the multi-ported memory independently (Fig. 1 Ref. 22).

As to claim 27, Dinwiddie discloses the invention as claimed above. Dinwiddie integrated circuit comprising a memory controller including at least two electrical ports for coupling to communication channel (Fig. 1)

As to claim 2, Dinwiddie discloses the invention as claimed above. Dinwiddie further discloses an OS is configured such that accesses to the multiported are not cached (Fig. 1).

As to claims 3 and 27, Dinwiddie discloses the invention as claimed. Dinwiddie further discloses the multi-ported memory is dual ported (Fig. 1 Ref. 22).

As to claim 4, Dinwiddie discloses the invention as claimed above. Dinwiddie further discloses the multiported memory is embedded within a memory controller (Fig. 1).

As to claim 5, Dinwiddie discloses the invention as claimed above. Dinwiddie further discloses the multiported memory and memory controller are integrated into a single chip (Fig. 1).

As to claims 6 and 29, Dinwiddie discloses the invention as claimed above. Dinwiddie further discloses DRAM (Fig. 13).

As to claim 9, Dinwiddie discloses the invention as claimed above. Dinwiddie further discloses I/O bus (Fig. 1 Ref. 16).

Claim Rejections - 35 USC § 103

13. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

14. Claims 7 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Camacho et al. (Camacho) US Patent 6,167,487, Csoppenszky et al. (Csoppenszky) US Patent 5,852,608, or Dinwiddie, Jr. et al. (Dinwiddie) US Patent 5,852,608 in view of McMahon et al (McMahon) US Patent 5,784,699.

As to claims 7 and 30, Camacho, Csoppenszky, or Dinwiddie discloses the invention as claimed above. However, neither Camacho, Csoppenszky, nor Dinwiddie specifically discloses reservation bits mapped to block of general purpose memory in the multiported memory. McMahon discloses reservation bits mapped to block of general purpose memory in the multiported memory (Fig. 3A) for the purpose of providing fast search and allocation/dealloction of availability of a block (col. 3 lines 7-26).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate reservation bits mapped to block of general purpose memory in the multiported memory as shown in McMahon into the invention of Camacho, Csoppenszky, or Dinwiddie because it would provide fast search and allocation/dealloction of availability of a block.

15. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are

such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

16. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Camacho et al. (Camacho) US Patent 6,167,487, Csoppenszky et al. (Csoppenszky) US Patent 5,852,608, or Dinwiddie, Jr. et al. (Dinwiddie) US Patent 5,852,608 in view of Young et al (Young) US Patent 5,546,554.

As to claim 8, Camacho, Csoppenszky, or Dinwiddie discloses the invention as claimed above. However, neither Camacho, Csoppenszky, nor Dinwiddie specifically discloses virtual addresses within multiported are mapped to physical address with smart addressing. Young discloses virtual addresses within multiported are mapped to physical address with smart addressing (Fig. 5a) for the purpose of memory that appears to an application to be larger and more uniform than it is.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate virtual addresses within multiported are mapped to physical address with smart addressing as shown in Young into the invention of Camacho, Csoppenszky, or Dinwiddie because it would provide capability of memory that appears to an application to be larger and more uniform than it is.

Claim Rejections - 35 USC § 103

17. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

18. Claims 10-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dinwiddie, Jr. et al. (Dinwiddie) US Patent 5,852,608 or Chin et al. (Chin) US Patent 6,167,487 in view of McMahon et al (McMahon) US Patent 5,784,699.

As to claim 10, Dinwiddie discloses a method comprising: making, from a peripheral device, a data access to memory in a computer (Fig. 1) and routing the data access to a first memory in the computer (Fig. 1 Ref. 7). However, Dinwiddie does not specifically disclose the steps of making from the peripheral device, a status access to memory in the computer and routing the status access to a second memory in the computer. McMahon discloses making from the peripheral device, a status access to memory in the computer and routing the status access to a second memory in the computer (Fig. 1) for the purpose of providing fast search and allocation/dealloction of availability of a memory block (col. 3 lines 7-26).
Alternatively, Chin discloses a method comprising: making, from a peripheral a data access to memory in a computer (Fig. 1 Ref. 20) and routing the data access to a first memory in the computer (Fig. 1 Refs. 18 and 30). However, Chin does not specifically disclose the steps of making from the peripheral device, a status access to memory in the computer and routing the status access to a second memory in the computer. McMahon discloses making from the peripheral device, a status access to memory in the computer and routing the status access to a

second memory in the computer (Fig. 1) for the purpose of providing fast search and allocation/dealloction of availability of a memory block (col. 3 lines 7-26).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate making from the peripheral device, a status access to memory in the computer and routing the status access to a second memory in the computer as shown in McMahon into the invention of Dinwiddie or Chin because it would provide fast search and allocation/dealloction of availability of a memory block.

As to claim 11, Dinwiddie, Chin, and McMahon disclose the invention as claimed above. Dinwiddie further discloses main memory (Fig. 1 Ref. 7). Chin further discloses main memory (Fig. 1 Refs. 18 and 32).

As to claim 12, Dinwiddie, Chin, and McMahon disclose the invention as claimed above. Dinwiddie further discloses the second memory comprises memory included in a memory controller (Fig. 1 Ref 22). Chin further discloses the second memory comprises memory included in a memory controller (Fig. 1 Refs. 20 and 15).

As to claim 13, Dinwiddie, Chin, and McMahon disclose the invention as claimed above. Dinwiddie further discloses dual ported (Fig. 1 Ref. 22). Chin further discloses dual ported (Fig. 1 Ref. 20).

As to claims 14 and 16-18, claims 14, and 16-18 are a rephrasing of claims 10-13 in a computer software form. The claims are rejected for the same reason as set forth above in claims

As to claim 15, Dinwiddie, Chin, and McMahon disclose the invention as claimed above. Dinwiddie further discloses I/O controller (Fig. 1 Ref. 2). Chin further discloses I/O controller (Fig. 1 Ref. 16).

As to claim 19, Dinwiddie discloses a method comprising: making, from a CPU, a data access to memory in a computer (Fig. 1) and routing the data access to a first memory in the computer (Fig. 1 Ref. 7). However, Dinwiddie does not specifically disclose the steps of making from the CPU, a status access to memory in the computer and routing the status access to a second memory in the computer. McMahon discloses making from the CPU, a status access to memory in the computer and routing the status access to a second memory in the computer (Fig. 1) for the purpose of providing fast search and allocation/dealloction of availability of a memory block (col. 3 lines 7-26).

Alternatively, Chin discloses a method comprising: making, from a CPU a data access to memory in a computer (Fig. 1 Ref. 20) and routing the data access to a first memory in the computer (Fig. 1 Refs. 18 and 30). However, Chin does not specifically disclose the steps of making from the CPU, a status access to memory in the computer and routing the status access to

a second memory in the computer. McMahon discloses making from the CPU, a status access to memory in the computer and routing the status access to a second memory in the computer (Fig. 1) for the purpose of providing fast search and allocation/dealloction of availability of a memory block (col. 3 lines 7-26).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate making from the CPU, a status access to memory in the computer and routing the status access to a second memory in the computer as shown in McMahon into the invention of Dinwiddie or Chin because it would provide fast search and allocation/dealloction of availability of a memory block.

As to claim 20, Dinwiddie, Chin, and McMahon disclose the invention as claimed above. Dinwiddie further discloses main memory (Fig. 1 Ref. 7). Chin further discloses main memory (Fig. 1 Refs. 18 and 32).

As to claim 21, Dinwiddie, Chin, and McMahon disclose the invention as claimed above. Dinwiddie further discloses the second memory comprises memory included in a memory controller (Fig. 1 Ref 22). Chin further discloses the second memory comprises memory included in a memory controller (Fig. 1 Refs. 20 and 15).

As to claim 22, Dinwiddie, Chin, and McMahon disclose the invention as claimed above.

Dinwiddie further discloses dual ported (Fig. 1 Ref. 22). Chin further discloses dual ported (Fig. 1 Ref. 20).

As to claims 23- 26, claims 23-26 are a rephrasing of claims 19-22 in a computer software form. The claims are rejected for the same reason as set forth above in claims

Conclusion

19. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. See attached PTO-892.

20. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) days from the mail date of this letter. Failure to respond within the period for response will result in **ABANDONMENT** of the application (see 35 USC 133, MPEP 710.02, 710.02(b)).

21. When responding to the office action, Applicant is advised to clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. He or she must also show how the amendments avoid such references or objections. See 37 C.F.R. § 1.111(c).

22. When responding to the office action, Applicants are advised to provide the examiner

with the line numbers and page numbers in the application and/or references cited to assist examiner to locate the appropriate paragraphs.

23. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Hong Kim whose telephone number is (703) 305-3835. The Examiner can normally be reached on the weekdays from 8:30 AM to 5:00 PM.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Do Yoo, can be reached on (703) 308-4908.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-3800.

24. **Any response to this action should be mailed to:**

Commissioner of Patents and Trademarks
Washington, D.C. 20231

or faxed to TC-2100:
After-final (703) 746-7238
Official (703) 746-7239 (for formal communications intended for entry)

Non-Official/Draft (703) 746-7240 (for informal or draft communications, please label "PROPOSED" or "DRAFT")

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington. VA., Sixth Floor (Receptionist).

HK
Primary Patent Examiner
May 16, 2002